REMARKS

Claims 1-3, 7-8, and 11-23 are all the claims presently pending in the application. Claims 3, 7-8, 11-12, 15, 17, and 20 are amended to more clearly define the invention and claims 4-6 and 9-10 are canceled. Claims 1, and 22-23 are independent.

These amendments are made only to more particularly point out the invention for the Examiner and not for narrowing the scope of the claims or for any reason related to a statutory requirement for patentability.

Applicant also notes that, notwithstanding any claim amendments herein or later during prosecution, Applicant's intent is to encompass equivalents of all claim elements.

Claims 1-3, 7-12, 19, and 22 - 23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the Yamane, et al. reference (U.S. Pat. No. 6,020,229) in view of the Chien, et al. reference (U.S. Pat. No. 6,432,768). Claims 13-18, and 20-21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the Yamane, et al. reference and the Chien, et al. reference and further in view of the Tsao, et al. reference (U.S. Pat. No. 6,143,594).

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

A first exemplary embodiment of the claimed invention, as defined by independent claim 1, is directed to a semiconductor device that includes a plurality of transistors including different gate insulator film in their thickness value. The plurality of transistors having different thickness values of a gate electrode thereof in correspondence to the thickness values of the gate insulator film thereof. The plurality of transistors include lightly doped

drain regions. The gate electrode includes an impurity to suppress depletion that is implanted when forming the lightly doped drain regions. The lightly doped drain regions have depths corresponding to the thickness values of the gate electrode and the gate insulator film.

A second exemplary embodiment of the claimed invention, as defined by independent claim 22, is directed to semiconductor device that includes a plurality of transistors having different gate insulator film thickness values. The plurality of types of transistors having different thickness values of a gate electrode thereof in correspondence to the thickness values of the gate insulator film thereof. The plurality of transistors include a plurality of sidewalls, a first lightly doped drain region, and a second lightly doped drain region. The first lightly doped drain region and the second lightly doped drain region are formed using the plurality of sidewalls and the gate electrode as a mask. The first and second lightly doped drain regions have depths corresponding to the thickness values of the gate electrode and the gate insulator film.

A third exemplary embodiment of the claimed invention, as defined by independent claim 23, is directed to semiconductor device that includes a plurality of transistors having different gate insulator film thickness values with a polysilicon film layer. The plurality of transistors having different thickness values of a gate electrode thereof in correspondence to the thickness values of the gate insulator film thereof. The thickness of the gate insulator film varies based on the amount of deposited gate electrode materials. The plurality of transistors include a plurality of sidewalls, and lightly doped drain regions formed using the plurality of sidewalls and the gate electrode as a mask. The lightly doped drain regions have depths corresponding to the thickness values of the gate electrode and the gate insulator film.

Conventional NMOSFET devices include the same gate electrode as a mask for both the core-purpose MOSFET and the I/O-purpose MOSFET. However, these devices restrict energy (ion) implantation into the lightly doped drain region making it very problematic to dope an impurity to a deep level thus forming shallow lightly doped drain regions with strong electric fields at the drains, which increase breakdown effects and give rise to hot carriers deteriorating the reliability of the device. (See Page 3, lines 3-8; Page 8, line 20-Page 9, line 5; Page 12, lines 1-10).

In stark contrast, the present invention includes a plurality of transistors with lightly doped drain region that have depths corresponding to the thickness values of the gate electrode and the gate insulator film. This feature reduces the electric field in the space region and efficiently suppresses the occurrence of a hot carrier and optimizes high-voltage reliability. (See Page 5, lines 1-10; Page 11, lines 8-11; Page 12, lines 1-10 and 20-24; Page 13, lines 1-7; Page 15, line 20-Page 16, line 11; and Figures 3(I)-(L)).

As a result, the claimed invention provides a semiconductor device with an increased process margin of the gate etching during manufacturing and improved performance. (See Page 5, lines 7-10; Page 12, lines 11-25).

II. THE PRIOR ART REJECTIONS

A. The Yamane et al. reference in view of the Chien et al. reference

The Examiner alleges that the Chien et al. reference would have been combined with the Yamane et al. reference to form the claimed invention. Applicant submits, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Applicant submits that these references would not have been combined as alleged by the Examiner. Indeed, the references are directed to completely different matters and problems.

Specifically, the Yamane et al. reference is directed to being able to form a resistance element that is thin enough to reduce parasitic capacitance but does not risk having contact holes that penetrate the resistance element (col. 2, lines 33-62).

In stark contrast, the Chien et al. reference is specifically directed to addressing the problem of having word lines for a logic circuit having a sufficiently low resistance without adversely affecting a memory device that is formed on the same chip (col. 1, lines 11-37).

One of ordinary skill in the art who was concerned with being able to form a resistance element that is thin enough to reduce parasitic capacitance but does not risk having contact holes that penetrate the resistance element as the Yamane et al. reference is concerned with solving would not have been referred to the Chien et al. reference because the Chien et al. reference is directed to the completely different and unrelated problem of having word lines for a logic circuits that have a sufficiently low resistance without adversely affecting a memory device that is formed on the same chip. Thus, the references would not have been combined by one of ordinary skill in the art.

Further, Applicant submits that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner. Indeed, the Examiner does not even support the combination by identifying a reason for combining the references.

The Examiner alleges that it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the semiconductor device disclosed by the Yamane et al. reference "to have Ldd regions since a Ldd structure performs functions of increasing the breakdown voltage, migrating of the hot carriers and inhibiting short channel effect."

However, the Examiner has failed to provide a *prima facie* case of obviousness by failing to provide a motivation to make the alleged combination.

Section 2141.01 of the Manual of Patent Examining Procedure (MPEP) requires:

> "When applying 35 U.S.C. 103, the following tenets of patent law must be adhered to: . . .
>
> (B) The references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination;" (emphasis added).

Further, section 2142 of the MPEP states:

> "To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings." (Emphasis added).

"To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in

the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings." (§ 2143, emphasis added)

"The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure." (M.P.E.P. § 2143.01, emphasis added).

"The mere fact that references can be combined or modified does not render the resultant combination unless the prior art also suggests the desirability of the combination." (Emphasis added, M.P.E.P. § 2143.01).

"There are three possible sources for a motivation to combine references; the nature of the problem to be solved, the teachings of the prior art, and the knowledge of persons of ordinary skill in the art.." (Id.).

The Examiner merely alleges a motivation without citing a source for the motivation or suggestion to make the alleged combination. As is clearly explained in the M.P.E.P., the Examiner is required to provide a citation for the alleged motivation or suggestion. Therefore, the Examiner's allegation of obviousness is clearly not sufficient to establish a *prima facie* case of obviousness.

To further the prosecution of this application, however, Applicant has closely reviewed the Yamane et al. reference and the Chien et al. reference to determine whether either of these references include a disclosure that explains, as alleged by the Examiner, that it would have been obvious to modify the semiconductor device disclosed by the Yamane et al. reference "to have Ldd regions since a Ldd structure performs functions of increasing the breakdown voltage, migrating of the hot carriers and inhibiting short channel effect."

Clearly, the Yamane et al. reference does not provide any disclosure of such an alleged motivation or suggestion to make such a modification. Indeed, as admitted by the Examiner, the Yamane et al. reference does not even disclose LDD regions, let alone any motivation or suggestion to provide LDD regions.

Similarly, the Chien et al. reference also fails to provide any disclosure of such an alleged motivation or suggestion to make such a modification. Rather, the Chien et al. reference merely peripherally mentions that ions may be implanted to form LDD regions at col. 2, lines 54-57 and col. 3, lines 17-19. However, while the Chien et al. reference appears to disclose LDD regions, the Chien et al. reference does not explain why the LDD regions are provided. Therefore, the Chien et al. reference also is not a source of the Examiner's alleged motivation or suggestion.

Thus, since neither of the applied references disclose the Examiner's alleged motivation or suggestion, the only remaining source which is available to the Examiner for alleging a *prima facie* case of obviousness is the knowledge generally available to one of ordinary skill in the art.

However, while the Examiner does not indicate that this is the source of the alleged motivation or suggestion, should the Examiner allege that the source is within the knowledge of one of ordinary skill in the art, Applicant hereby submits a "seasonable demand for evidence" (M.P.E.P. § 2144.03) and requests that the Examiner either 1) cite a reference in support of the Examiner's position; or 2) if the Examiner contends that the rejection is based upon facts within the personal knowledge of the Examiner, that the Examiner provide a Affidavit that sets forth the specific data and facts that supports the Examiner's position in accordance with the requirements of the M.P.E.P. § 2144.03.

"[A]ssertions of technical facts in areas of esoteric technology must always be supported by citation of some reference work and allegations regarding specific 'knowledge' of the prior art, which might be peculiar to a particular art should also be supported." (Emphasis added, M.P.E.P. § 2144.03).

Applicant notes that the Examiner's alleged motivation or suggestion to modify the Yamane et al. reference to include LDD regions based upon the disclosure of the Chien et al. reference is curiously similar to the advantages that are provided by Applicant's own disclosure (see, for example, page 4, line 24 - page 6, line 24). Clearly, as explained above and by the M.P.E.P., the Applicant's own disclosure is not available as a source for a motivation in a *prima facie* obviousness rejection (M.P.E.P. § 2143.01).

Moreover, even assuming arguendo that one of ordinary skill in the art would have been motivated to combine these references, the combination would not teach or suggest each and every element of the claimed invention.

The Examiner admits that the Yamane et al. reference does not teach or suggest LDD regions, let alone LDD regions that have depths corresponding to the thickness values of the gate electrode and the gate insulator film. As explained above, this feature reduces the electric field in the space region and efficiently suppresses the occurrence of a hot carrier and optimizes high-voltage reliability. As a result, the claimed invention provides a semiconductor device with an increased process margin of the gate etching during manufacturing and improved performance.

The Chien et al. reference does not remedy the deficiencies of the Yamane et al. reference. While the Chien et al. reference appears to disclose LDD regions at 116 and 132 in

Figs. 1D - 1F, the Chien et al. reference does not teach or suggest that the depths of these LDD regions correspond to the thickness values of the gate electrode and the gate insulator film.

Rather, as explained above, the Chien et al. reference merely discloses that the LDD regions 116 and 132 may be provided to the semiconductor device at col. 2, lines 54-57 and col. 3, lines 17-19. The Chien et al. reference does not teach that the depths of the LDD regions 116 and 132 correspond to the thickness values of the gate electrode and the gate insulator film. Indeed, the Chien et al. reference does not teach or suggest any relationship at all between the depth of the LDD regions 116 and 132 and the thicknesses of the gate electrode and the gate insulator film, let alone that the depth of these LDD regions 116 and 132 correspond to the thickness values of the gate electrode and the gate insulator film.

The Examiner alleges that the Chien et al. reference in Fig. 1F appears to disclose a thicker gate 112 with a deeper LDD region 116 and a thinner gate 124 with a shallow Ldd region 132. However, as explained above, even assuming arguendo that the Chien et al. reference discloses these features, the Chien et al. reference does not mention anything at all regarding any relationship between the depths of the LDD regions 116 and 132 and the thicknesses of the gate electrodes 112 and 124, let alone that the depths of the LDD regions 116 and 132 correspond to the thickness values of the gate electrode and the gate insulator film.

Further, the Examiner has not even alleged that there is any relationship at all between the depths of the LDD regions 116 and 132 and the thickness of the gate insulator film.

Additionally, the Examiner alleges that "It would be obvious that a deeper LDD region is formed with a thicker gate since the Ldd region of Chien (sic) is formed using a gate

as a mask. However, contrary to the Examiner's allegations, while the Chien et al. reference appears to disclose using the gate electrodes as a mask when forming the LDD regions 116 and 132, the Chien et al. reference does not teach or suggest that there is any relationship at all between the depth of the LDD regions 116 and 132 and the thickness of the gate electrodes 112 and 124, let alone a depth of the LDD region that corresponds to the thickness values of the gate electrode and the gate insulator film.

Lastly, even assuming arguendo that the Chien et al. reference does disclose a correspondence between the depths of the LDD regions and the thicknesses of the gate electrode and the gate insulator film, the Chien et al. reference does not teach or suggest any motivation or suggestion to make the depths of LDD regions correspond with the thicknesses of the gate electrode and the gate insulator film.

Therefore, the Examiner is respectfully requested to withdraw the rejection of claims 1-3, 5-6, 8-11 and 14-18.

B. The Yamane et al. reference in view of the Chien et al. reference and in further view of the Tsao et al. reference

The Examiner alleges that the Chien et al. reference would have been combined with the Yamane et al. reference and further that the Tsao et al. reference would have been combined with the Yamane et al. reference and the Chien et al. reference to form the claimed invention. Applicant submits, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Applicant submits that these references would not have been combined as alleged by the Examiner. Indeed, the references are directed to completely different matters and problems.

As explained above, one of ordinary skill in the art would not have combined the teachings of the Chien et al. reference with the teachings of the Yamane et al. reference because one of ordinary skill in the art who was concerned with being able to form a resistance element that is thin enough to reduce parasitic capacitance but does not risk having contact holes that penetrate the resistance element as the Yamane et al. reference is concerned with solving would not have been referred to the Chien et al. reference because the Chien et al. reference is directed to the completely different and unrelated problem of having word lines for a logic circuits that have a sufficiently low resistance without adversely affecting a memory device that is formed on the same chip.

In stark contrast to the Yamane et al. reference and the Chien et al. reference, the Tsao et al. reference is directed to the completely different and unrelated problem of providing protection against electrostatic discharge in mixed voltage IC chips (col. 1, lines 12-14) by providing a high-voltage NMOS transistor in an electrostatic discharge protection circuit that generates more substrate current in an electrostatic discharge event (col. 2, lines 45-49).

Therefore, one of ordinary skill in the art who was concerned with being able to form a resistance element that is thin enough to reduce parasitic capacitance but does not risk having contact holes that penetrate the resistance element as the Yamane et al. reference is concerned with solving or who was concerned with the problem of having word lines for a logic circuits that have a sufficiently low resistance without adversely affecting a memory device that is form d on the same chip as the Chien et al. reference is concerned with solving

would not have referred to the Tsao et al. reference to solve these problems because the Tsao et al. reference is concerned with the completely different and unrelated problem of providing protection against electrostatic discharge in mixed voltage IC chips. Thus, the references would not have been combined, absent hindsight.

Further, Applicant submits that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner. Indeed, the Examiner does not even support the combination by identifying a reason for combining the references.

Rather, the Examiner merely alleges that one of ordinary skill in the art to modify the semiconductor device that is disclosed in the Yamane et al. reference to include a NMOS device "since an NMOS is most commonly used for a semiconductor device." However, contrary to the Examiner's allegation, the mere fact that an NMOS device may be commonly used, does not provide a motivation or suggestion to modify the existing structure that is disclosed by the Yamane et al. reference.

As explained above, it is not sufficient to merely point out the existence of a feature in a secondary reference as a basis for making a modification. Rather, in order to establish a *prima facie* case of obviousness the Examiner must cite a reference that provides a motivation to modify the device disclosed in the Yamane et al. reference.

Similarly, the Examiner alleges that it would have been obvious to one of ordinary skill in the art to modify the semiconductor device that is disclosed by the Yamane et al. reference "in order to obtain proper operating voltages for electrical function of the device."

In other words, the Examiner is alleging that the semiconductor device that is disclosed by the Yamane et al. reference does not include "proper operating voltages for

electrical function of the device." Thus, the Examiner is contending that the semiconductor device that is disclosed by the Yamane et al. reference is not operable.

However, contrary to the Examiner's allegation, the Yamane et al. reference does not teach or suggest that the semiconductor device that is disclosed by the Yamane et al. reference is not operable.

Further, none of the other applied references (the Chien et al. reference and the Tsao et al. reference) also do not teach or suggest that the semiconductor device that is disclosed by the Yamane et al. reference is not operable.

Therefore, contrary to the Examiner's allegations, one of ordinary skill in the art would not have been motivated to modify the semiconductor device that is disclosed by the Yamane et al. references based upon the disclosure of the Tsao et al. reference in order to make the semiconductor device that is disclosed by the Yamane et al. reference operable.

Moreover, even assuming arguendo that one of ordinary skill in the art would have been motivated to combine these references, the combination would not teach or suggest each and every element of the claimed invention.

None of the applied references teaches or suggests the features of the claimed invention including a depth of the LDD region that corresponds to the thickness values of the gate electrode and the gate insulator film. As explained above, this feature reduces the electric field in the space region and efficiently suppresses the occurrence of a hot carrier and optimizes high-voltage reliability. As a result, the claimed invention provides a semiconductor device with an increased process margin of the gate etching during manufacturing and improved performance.

As explained above, neither of the Yamane et al. and Chien et al. references teach or suggest the feature of a depth of the LDD region that corresponds to the thickness values of the gate electrode and the gate insulator film.

The Tsao et al. reference does not remedy this deficiency.

Therefore, the Examiner is respectfully requested to withdraw the rejection of claims 13-18 and 20-21.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing amendments and remarks, Applicant respectfully submits that claims 1-3, 7-8, and 11-23, all the claims presently pending in the Application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the Application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 1/9/04

James E. Howard
Registration No. 39,715

McGinn & Gibb, PLLC
8321 Old Courthouse Rd., Suite 200
Vienna, Virginia 22182
(703) 761-4100
Customer No. 21254

CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that I am filing this Amendment by facsimile with the United States Patent and Trademark Office to Examiner Im, Junghwa M., Group Art Unit 2811 at fax number (703) 872-9306 this 9th day of January, 2004.

James E. Howard
Reg. No. 39,715